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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/854,543	05/14/2001	Allen King	MLX920000005US1	8324

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EXAMINER

DUNCAN, MARC M

ART UNIT	PAPER NUMBER
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2113

5

DATE MAILED: 04/06/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/854,543

Applicant(s)

KING ET AL.

Examiner

Marc M Duncan

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 14 May 2001.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-29 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-4, 6-8, 10-15, 17-19, 21-24 and 27-29 is/are rejected.
- 7) ☒ Claim(s) 5, 9, 16, 20, 25 and 26 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 14 May 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 2.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

Status of the Claims

Claim 27 is rejected under 35 USC 102(b).

Claims 23-24 are rejected under 35 USC 102(e).

Claims 1, 2, 3, 4, 6, 7, 8, 10, 11, 12, 13, 14, 15, 17, 18, 19, 21, 22, 28 and 29 are rejected under 35 USC 103(a).

Claims 5, 9, 16, 20, 25 and 26 are objected to.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 23-24 are rejected under 35 U.S.C. 102(e) as being anticipated by Peters et al.

Regarding claim 23:

Peters teaches an error table disposed in a storage controller, the error table configured with addresses for data error locations on a storage device so that for a write request, the storage controller knows to perform a write and verify command to transfer the data to the storage device and to verify the successful transfer of the data to the storage device in col. 4 line 64-col. 5 line 1 and col. 5 lines 7-9. The examiner has

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determined that the reallocation table with flags taught by Peters is equivalent to the recited error table.

Regarding claim 24:

Peters teaches a write recovery bit to indicate when an address associated therewith requires a write recovery during a write in col. 4 line 64-col. 5 line 1.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 27 is rejected under 35 U.S.C. 102(b) as being anticipated by Nagaraj et al.

Regarding claim 27:

Nagaraj teaches a memory configured for storing an error table and data fields, the error table comprising a non-volatile array configuration information storage area in col. 3 lines 46-64 and Fig. 8.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1, 2, 3, 4, 6, 7, 8, 10, 11, 12, 13, 14, 15, 17, 18, 19, 21, 22, 28 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tillson in view of Peters et al.

Regarding claim 1:

Tillson teaches issuing a command to write and verify data transfer when requested to write to a specified location address in the Abstract lines 3-7, col. 2 lines 58-65 and col. 3 lines 4-9.

Tillson teaches reassigning the data to a new location address when the command to write and verify the data transfer is unsuccessful in the Abstract lines 8-12 and col. 3 lines 10-20.

Tillson does not explicitly teach the location address stored in an error table. Tillson does, however, teach verifying writes to specified locations in order to detect errors that are permanent.

Peters teaches issuing a command to write and verify to a location address stored in an error table in col. 4 line 64-col. 5 line 1 and col. 5 lines 7-9. The examiner

has determined that the reallocation table with flags of Peters is equivalent to the recited error table.

It would have been obvious to one of ordinary skill in the art at the time of invention to combine the table teaching of Peters with the write and verify teaching of Tillson.

One of ordinary skill in the art at the time of invention would have been motivated to combine the teachings because Tillson discloses that performing a write and verify on every location address could cause performance penalties. By only causing a write and verify on locations specified to be in error, as taught by Peters, the need of eliminating performance penalties expressed by Tillson is solved.

Tillson and Peters do not explicitly teach a non-redundant disk array storage system. Tillson and Peters do, however, teach hard disk drives.

The examiner takes official notice that a non-redundant disk array was well known at the time of invention.

It would have been obvious to one of ordinary skill in the art at the time of invention to combine the hard drives of Tillson and Peters with a non-redundant disk array storage system.

One of ordinary skill in the art at the time of invention would have been motivated to combine the teachings because a non-redundant disk array storage system is composed of hard drives such as those taught by Peters and Tillson. Non-redundant disk arrays were commonly used by those of ordinary skill in the art at the time of invention to provide a larger amount of storage than a single hard drive could offer.

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Regarding claim 2:

Peters teaches wherein the error table recording error locations on a disk drive in col. 4 line 64-col. 5 line 1.

Regarding claim 3:

Tillson teaches transferring the data to the specified location address when a good status is returned in response to the command to write and verify the data transfer in col. 2 lines 58-65.

Regarding claim 4:

Peters teaches wherein the error table comprises a write recovery table in col. 4 line 64-col. 5 line 1. The determined that the table of Peters contains a flag for locations that require special treatment when writing in order to determine the presence of an unrecoverable error, which is equivalent to the teaching of a write recovery table.

Regarding claim 6:

Peters teaches wherein the command to write and verify the data transfer comprises a write/verify command in col. 5 lines 7-9.

Regarding claim 7:

Tillson teaches wherein the command to write and verify the data transfer comprises a write command followed by a read command with the force unit access bit being set to 1 to force the data to be read from the disk drive rather than from the disk drive cache in col. 2 lines 58-65 and col. 3 lines 4-9. It is inherent in the teaching of Tillson for the force unit access bit to be set to 1. In order to verify the data written to the data sectors it is necessary to read from the drive rather than the cache.

Regarding claim 8:

Tillson teaches wherein the command to write and verify the data transfer is unsuccessful only when a predetermined number of write and verify retries is exhausted in the Abstract lines 8-12 and col. 3 lines 10-20.

Regarding claim 10:

Peters teaches deleting the specified location address that is stored in the error table when the reassign of data is successful in col. 4 lines 37-56.

Regarding claim 11:

Peters teaches deleting the specified location address that is stored in the error table when the command to write and verify the data transfer is successful in col. 5 lines 1-2.

Regarding claim 12:

Tillson teaches a storage controller in col. 2 line 61.

Tillson teaches the storage controller being configured to issue a command to write and verify data transfer when requested to write data to a specified location address and reassign the data to a new location address when the command to write and verify the data transfer is unsuccessful in the Abstract lines 3-12, col. 2 lines 58-65 and col. 3 lines 4-20.

Tillson does not explicitly teach the location address stored in an error table. Tillson does not explicitly teach the storage controller including a memory for maintaining an error table. Tillson does, however, teach verifying writes to specified locations in order to detect errors that are permanent.

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Peters teaches issuing a command to write and verify to a location address stored in an error table in col. 4 line 64-col. 5 line 1 and col. 5 lines 7-9. Peters teaches the storage controller including a memory for maintaining an error table in col. 4 lines 64-col. 5 line 1 and col. 5 lines 7-9. The examiner has determined that the reallocation table with flags that is taught by Peters is equivalent to the recited error table.

It would have been obvious to one of ordinary skill in the art at the time of invention to combine the table teaching of Peters with the write and verify teaching of Tillson.

One of ordinary skill in the art at the time of invention would have been motivated to combine the teachings because Tillson discloses that performing a write and verify on every location address could cause performance penalties. By only causing a write and verify on locations specified to be in error, as taught by Peters, the need of eliminating performance penalties expressed by Tillson is solved.

Tillson and Peters do not explicitly teach an array of storage devices. Tillson and Peters do, however, teach hard disk drives.

The examiner takes official notice that a non-redundant disk array was well known at the time of invention.

It would have been obvious to one of ordinary skill in the art at the time of invention to combine the hard drives of Tillson and Peters with an array of storage devices.

One of ordinary skill in the art at the time of invention would have been motivated to combine the teachings because an array of storage devices is composed of hard

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drives such as those taught by Peters and Tillson. An array of storage devices was commonly used by those of ordinary skill in the art at the time of invention to provide a larger amount of storage than a single hard drive could offer.

Regarding claim 13:

Peters teaches wherein the error table recording error locations on a disk drive in col. 4 line 64-col. 5 line 1.

Regarding claim 14:

Tillson teaches transferring the data to the specified location address when a good status is returned in response to the command to write and verify the data transfer in col. 2 lines 58-65.

Regarding claim 15:

Peters teaches wherein the error table comprises a write recovery table in col. 4 line 64-col. 5 line 1. The determined that the table of Peters contains a flag for locations that require special treatment when writing in order to determine the presence of an unrecoverable error, which is equivalent to the teaching of a write recovery table.

Regarding claim 17:

Peters teaches wherein the command to write and verify the data transfer comprises a write/verify command in col. 5 lines 7-9.

Regarding claim 18:

Tillson teaches wherein the command to write and verify the data transfer comprises a write command followed by a read command with the force unit access bit being set to 1 to force the data to be read from the disk drive rather than from the disk

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drive cache in col. 2 lines 58-65 and col. 3 lines 4-9. It is inherent in the teaching of Tillson for the force unit access bit to be set to 1. In order to verify the data written to the data sectors it is necessary to read from the drive rather than the cache.

Regarding claim 19:

Tillson teaches wherein the command to write and verify the data transfer is unsuccessful only when a predetermined number of write and verify retries is exhausted in the Abstract lines 8-12 and col. 3 lines 10-20.

Regarding claim 21:

Peters teaches deleting the specified location address that is stored in the error table when the reassign of data is successful in col. 4 lines 37-56.

Regarding claim 22:

Peters teaches deleting the specified location address that is stored in the error table when the command to write and verify the data transfer is successful in col. 5 lines 1-2.

Regarding claim 28:

The claim is rejected as the article of manufacture containing computer executable instructions that cause the method of claim 1 to be performed.

Regarding claim 29:

See the teachings cited above for claim 1.

Peters also teaches recording read error locations in an error table in col. 4 line 64-col. 5 line 1.

Allowable Subject Matter

Claims 5, 9, 16, 20, 25 and 26 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: Prior art was not found that explicitly teaches or fairly suggests the error table comprising a combined write recovery table and bad data table as outlined in claims 5 and 16. Prior art was not found that explicitly teaches or fairly suggests returning a fatal error status and marking the disk offline after a predetermined number retries is exhausted for the process of reassigning data after detecting an error as outlined in claims 9 and 20. Prior art was not found that explicitly teaches or fairly suggests the write recovery bit allowing a bad data table to be combined with the write recovery table as outlined in claim 25. These limitations are considered allowable only when taken in combination with all limitations of the base claim and any intervening claims.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The prior art not relied upon contains elements of the instant claims and/or represents a current state of the art.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Marc M Duncan whose telephone number is 703-305-4622. The examiner can normally be reached on M-T and TH-F 6:00-4:30.


If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on 703-305-9713. The fax phone

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number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

md


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